
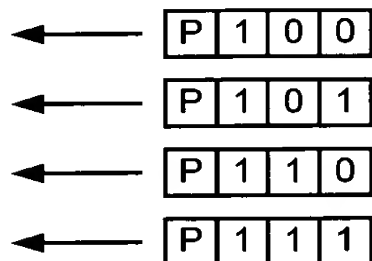


The diagram illustrates a Bi-directional Serial Link (14) connecting a Peripheral (Transmitter) (10) and a Card (Receiver) (12). The Peripheral (Transmitter) (10) outputs signals VC0, VC1, VC2, VC3, VC4, and VCN to the Bi-directional Serial Link (14). The Card (Receiver) (12) outputs signals to the Bi-directional Serial Link (14).

## CONTROL CHARACTERS



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- FLOW CONTROL CHARACTER (FCC)
- END OF HEADER (EOH)
- END OF PACKET (EOP)
- ESCAPE (ESC)

## DATA PACKET FORMAT

3 bits	0 to 65,536 bytes	3 bits	0 to 65,536 bytes	1 byte
EOP	Data	EOH	Header	VCN

## CREDIT PACKET FORMAT

3 bits	3 bits	8 bits
ESC	EOH	VCN

FIG. 2

00535696-032700

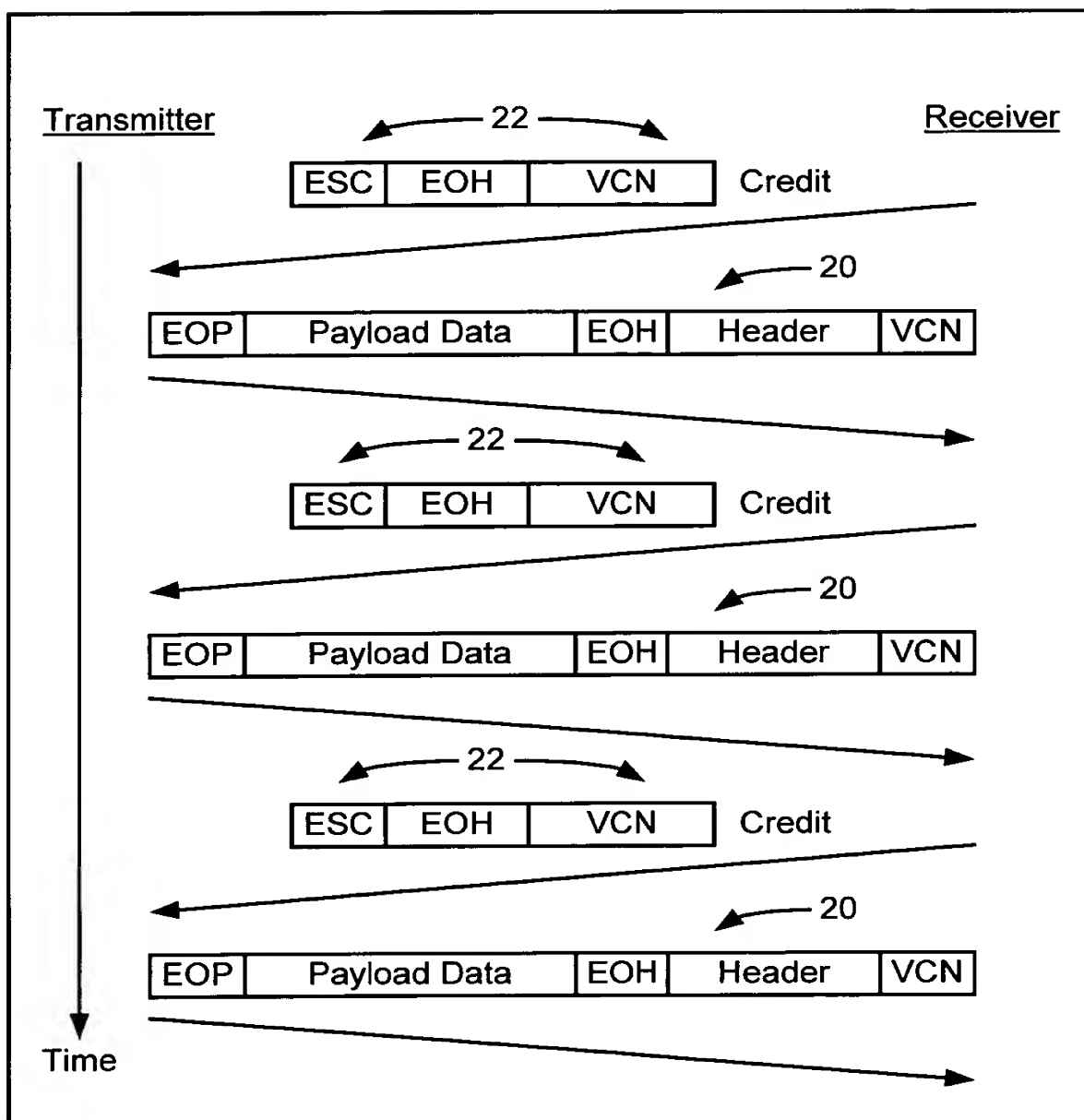


FIG. 3

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graph TD
    28([START RECEIVER PROCESS]) --> 30{{COMMUNICATION LINK ESTABLISHED}}
    30 --> 32[SPAWN A RECEIVER PROCESS]
    32 --> 34[RECEIVER CHECKS FOR AVAILABLE BUFFER FOR VCN "N"]
    34 --> 36{AVAILABLE BUFFER?}
    36 -- NO --> WAIT1[WAIT]
    WAIT1 --> 34
    36 -- YES --> 38[RECEIVER SEND A VC CREDIT PACKET FOR VCN "N" TO TRANSMITTER]
    38 --> 40{DATA PACKET RECEIVED ON VCN "N"?}
    40 -- NO --> WAIT2[WAIT]
    WAIT2 --> 40
    40 -- YES --> 41[DATA PACKET RECEIVED]
    41 --> 42[REPEAT FOR VCN "N+1" UNTIL ALL VCNS ARE RUNNING]
    42 --> 28
    42 --> 44([EXIT])
  
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FIG. 4

FIG. 4

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graph TD
    46([START TRANSMITTER PROCESS]) --> 48{{COMMUNICATION LINK ESTABLISHED}}
    48 --> 50[SPAWN A TRANSMITTER PROCESS FOR VCN]
    50 --> 52[TRANSMITTER CHECKS FOR AVAILABLE BUFFER FOR VCN "N"]
    52 --> 54{AVAILABLE BUFFER?}
    54 -- NO --> WAIT1[WAIT]
    WAIT1 --> 52
    54 -- YES --> 56{VC CREDIT RECEIVED FOR VCN N?}
    56 -- NO --> WAIT2[WAIT]
    WAIT2 --> 56
    56 -- YES --> 58{DATA PACKET?}
    58 -- NO --> WAIT3[WAIT]
    WAIT3 --> 58
    58 -- YES --> 60[TRANSMIT A PACKET]
    60 --> 62[REPEAT FOR VCN "N+1" UNTIL ALL VCNS ARE RUNNING]
    62 --> 46
    62 --> 64([EXIT])
  
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FIG. 5

FIG. 5